MATH LOVE INSTITUTE

Raipur, Chhattisgarh

Education as a Service (EaaS)

📞 Contact: www.mathlove.in | 📧 Specialized CBSE Coaching

Class 12 Physics - Chapter 14: SEMICONDUCTOR ELECTRONICS

🔌 SEMICONDUCTOR ELECTRONICS

📌 Chapter Overview

Welcome to the fascinating world of semiconductor electronics - the foundation of modern technology!

- ⚛️ Classification of Materials (Conductors, Semiconductors, Insulators)
- 📊 Energy Band Theory
- 💎 Intrinsic and Extrinsic Semiconductors
- 🔗 p-n Junction and Diode
- 📈 V-I Characteristics of Diodes
- 💡 Applications: Rectifiers, Zener Diode, LED, Photodiode, Solar Cell
- 🕴️ Transistors (BJT) - Structure and Working
- 🔊 Transistor as Amplifier and Switch
- 🚪 Logic Gates and Integrated Circuits

⚡ 1. INTRODUCTION TO SEMICONDUCTORS

🔑 Classification of Materials Based on Conductivity

Type	Resistivity (Ω·m)	Examples	Band Gap (eV)
Conductors	10^{-8} to 10^{-6}	Cu, Ag, Al, Au	Overlapping bands
Semiconductors	10^{-4} to 10^{5}	Si, Ge, GaAs	~1 eV (Si: 1.1, Ge: 0.7)
Insulators	10^{11} to 10^{17}	Glass, Rubber, Wood	> 3 eV (Diamond: 6)

📊 Energy Band Theory

🎯 Formation of Energy Bands

Isolated Atom:

- Electrons occupy discrete energy levels
- Each level can hold limited electrons ($2n^2$)

When Atoms Come Together:

- Energy levels split into closely spaced sub-levels
- In solid: N atoms create N closely spaced levels
- These form continuous energy bands

Three Important Regions:

1. **Valence Band (VB):** Highest occupied energy band at 0 K
2. **Forbidden Gap (E_g):** Energy gap between VB and CB
3. **Conduction Band (CB):** Lowest unoccupied energy band

💡 Energy Band Characteristics

Material	Valence Band	Conduction Band	Energy Gap	Conductivity at 0 K
Conductor	Partially filled or overlaps with CB	Overlaps with VB	$E_g = 0$	High
Semiconductor	Completely filled	Empty	$E_g \sim 1$ eV	Zero (increases with T)
Insulator	Completely filled	Empty	$E_g > 3$ eV	Zero (remains low)

💎 2. INTRINSIC SEMICONDUCTORS

🔑 Pure Semiconductors

Definition: Pure semiconductor without any impurity atoms

Common Examples:

- **Silicon (Si):** Most widely used (E_g = 1.1 eV)
- **Germanium (Ge):** Earlier used (E_g = 0.7 eV)
- Both are Group IV elements with 4 valence electrons

Crystal Structure:

- Each atom forms 4 covalent bonds with neighbors
- Diamond cubic lattice structure
- All bonds satisfied at 0 K - perfect insulator

🌡️ Temperature Effect on Intrinsic Semiconductors

⚡ Charge Carrier Generation

At 0 K (Absolute Zero):

- All bonds are intact
- No free electrons - acts as insulator
- Valence band completely filled
- Conduction band completely empty

At Room Temperature (300 K):

- Thermal energy breaks some covalent bonds
- **Free electrons:** Jump to conduction band
- **Holes:** Created in valence band (positive charge carriers)
- Number of electrons = Number of holes ($n_i = p_i$)

$n_i = p_i$ = Intrinsic Carrier Concentration

For Si at 300 K: $n_i \approx 1.5 \times 10^{10}$ cm^{-3}

For Ge at 300 K: $n_i \approx 2.5 \times 10^{13}$ cm^{-3}

🔄 Current in Intrinsic Semiconductors

Two Types of Current:

1. Electron Current:

- Free electrons in conduction band
- Move opposite to electric field
- Negative charge carriers

2. Hole Current:

- Vacancies in valence band
- Move in direction of electric field
- Positive charge carriers
- Actually electrons jumping to fill holes

Total Current = Electron Current + Hole Current

$$I = I_e + I_h$$

🔬 3. EXTRINSIC SEMICONDUCTORS (DOPED)

🎯 Doping Process

Definition: Addition of impurity atoms to pure semiconductor to increase conductivity

Purpose:

- Increase number of charge carriers
- Control type of majority carriers
- Enhance conductivity by orders of magnitude

Doping Level:

- Typically 1 impurity atom per 10^6 to 10^8 atoms
- Increases carrier concentration from 10^{10} to 10^{17} cm^{-3}

⚡ n-Type Semiconductor

🔋 Donor Impurity (Group V Elements)

Dopants: Phosphorus (P), Arsenic (As), Antimony (Sb) - 5 valence electrons

Doping Mechanism:

- Group V atom replaces Si/Ge atom
- 4 electrons form covalent bonds
- 5th electron is loosely bound (donor level)
- Easily donated to conduction band

Characteristics:

- **Majority carriers:** Electrons (negative)
- **Minority carriers:** Holes
- $n_e >> n_h$
- Overall charge: Neutral (donor ions are positive)

n-type: Electron Concentration >> Hole Concentration

$n_e \approx N_D$ (donor concentration)

p-Type Semiconductor

Acceptor Impurity (Group III Elements)

Dopants: Boron (B), Aluminum (Al), Gallium (Ga), Indium (In) - 3 valence electrons

Doping Mechanism:

- Group III atom replaces Si/Ge atom
- Only 3 electrons available for 4 bonds
- Creates hole (acceptor level)
- Accepts electron from valence band

Characteristics:

- **Majority carriers:** Holes (positive)
- **Minority carriers:** Electrons
- $n_h >> n_e$
- Overall charge: Neutral (acceptor ions are negative)

p-type: Hole Concentration >> Electron Concentration

$n_h \approx N_A$ (acceptor concentration)

📊 Comparison: n-type vs p-type

Property	n-Type	p-Type
Dopant	Group V (P, As, Sb)	Group III (B, Al, Ga)
Valence electrons	5	3
Majority carriers	Electrons (negative)	Holes (positive)
Minority carriers	Holes	Electrons
Impurity level	Donor level (near CB)	Acceptor level (near VB)
Current mainly due to	Electron flow	Hole flow
Fermi level	Near conduction band	Near valence band

🔗 4. p-n JUNCTION DIODE

🎯 Formation of p-n Junction

Definition: Interface formed by joining p-type and n-type semiconductors

Formation Process:

1. **Initially:** p-side has holes, n-side has electrons
2. **Diffusion:** Holes diffuse from p to n, electrons from n to p
3. **Recombination:** Carriers recombine near junction
4. **Depletion Region:** Region depleted of mobile charge carriers
5. **Space Charge:** Immobile ions create electric field

⚡ Depletion Region

🔬 Key Characteristics

Depletion Layer:

- Width: Typically 0.5 μm to 1 μm
- Contains immobile ions only (no mobile carriers)
- **p-side:** Negative acceptor ions (immobile)
- **n-side:** Positive donor ions (immobile)

Barrier Potential (V_0):

- Potential difference across junction
- **Silicon:** $V_0 \approx 0.7$ V
- **Germanium:** $V_0 \approx 0.3$ V
- Prevents further diffusion at equilibrium

Barrier Potential

$$V_0 = (kT/e) \ln(N_A N_D / n_i^2)$$

At room temperature (300 K): $kT/e \approx 26$ mV

🔌 Biasing of p-n Junction

⚡ Forward Bias

Connection: Positive terminal to p-side, negative to n-side

Effects:

- Applied voltage opposes barrier potential
- Depletion region width decreases
- Barrier potential reduced: $V_B = V_0 - V$ (V = applied voltage)
- **If $V > V_0$:** Large current flows (diode conducts)
- Resistance: Very low (~ few ohms)

Forward Bias: Diode ON

Current flows when V > 0.7 V (Si) or V > 0.3 V (Ge)

⚡ Reverse Bias

Connection: Negative terminal to p-side, positive to n-side

Effects:

- Applied voltage aids barrier potential
- Depletion region width increases
- Barrier potential increased: $V_B = V_0 + V$
- Very small reverse saturation current I_0 (μA to nA)
- Resistance: Very high (~ MΩ)

Breakdown:

- At very high reverse voltage (> breakdown voltage)
- Sudden increase in reverse current
- Can damage diode if not controlled

Reverse Bias: Diode OFF

Only small leakage current I_0 flows

📈 V-I Characteristics of p-n Junction Diode

📊 Current-Voltage Relationship

Diode Current Equation:

$$I = I_0[e^{eV/kT} - 1]$$

I_0 = Reverse saturation current

e = Electronic charge (1.6×10^{-19} C)

k = Boltzmann constant (1.38×10^{-23} J/K)

T = Absolute temperature (K)

V = Applied voltage

Key Observations:

Forward Bias (V > 0):

- When $V \ll kT/e$: Current ≈ 0 (very small)
- When $V \approx V_0$ (threshold): Current starts increasing
- When $V > V_0$: Current increases exponentially
- **Threshold voltage:** 0.7 V (Si), 0.3 V (Ge)

Reverse Bias (V < 0):

- Small constant current $I \approx -I_0$
- I_0 depends on temperature (doubles for every 10°C rise)
- At breakdown voltage: Sudden large increase

🔑 Important Parameters

Parameter	Silicon (Si)	Germanium (Ge)
Band gap E_g	1.1 eV	0.7 eV
Barrier potential V_0	0.7 V	0.3 V
Forward voltage drop	~0.7 V	~0.3 V
Reverse saturation current	~ nA	~ μA
Max operating temp	~200°C	~85°C

💡 5. APPLICATIONS OF JUNCTION DIODE

🔄 Rectifier - AC to DC Conversion

⚡ Half-Wave Rectifier

Circuit: Single diode + Load resistor

Working:

- **Positive half cycle:** Diode forward biased → conducts
- **Negative half cycle:** Diode reverse biased → blocks
- Output: Only positive half cycles appear

Characteristics:

- **Efficiency:** 40.6%
- **Ripple factor:** 1.21 (high - poor filtering)
- **Output DC:** $V_{dc} = V_m/\pi$
- **PIV:** V_m (Peak Inverse Voltage)

⚡ Full-Wave Rectifier (Center-Tap)

Circuit: Two diodes + Center-tapped transformer + Load

Working:

- Each diode conducts for alternate half cycles
- Both half cycles contribute to output
- Current always flows in same direction through load

Characteristics:

- **Efficiency:** 81.2% (double of half-wave)
- **Ripple factor:** 0.48 (better than half-wave)
- **Output DC:** $V_{dc} = 2V_m/\pi$
- **PIV:** $2V_m$

⚡ Full-Wave Bridge Rectifier

Circuit: Four diodes in bridge configuration + Load

Advantages over Center-Tap:

- No need for center-tapped transformer
- Better transformer utilization
- PIV = V_m (half of center-tap)
- Most commonly used configuration

Characteristics:

- **Efficiency:** 81.2%
- **Ripple factor:** 0.48
- **Output DC:** $V_{dc} = 2V_m/\pi$
- **PIV:** V_m

📊 Rectifier Comparison

Parameter	Half-Wave	Full-Wave (Center-Tap)	Bridge
Number of diodes	1	2	4
Transformer	Ordinary	Center-tapped	Ordinary
Efficiency	40.6%	81.2%	81.2%
Ripple factor	1.21	0.48	0.48
V_{dc}	V_m/π	$2V_m/\pi$	$2V_m/\pi$
PIV per diode	V_m	$2V_m$	V_m

⚡ Zener Diode - Voltage Regulator

🔧 Special Purpose Diode

Key Feature: Operates in reverse breakdown region

Characteristics:

- Sharp breakdown at specific voltage (Zener voltage V_Z)
- Voltage remains constant in breakdown region
- Current can vary widely without voltage change
- Available in range: 2.4 V to 200 V

Voltage Regulator Circuit:

- Connected in reverse bias across load
- Series resistor R_S limits current
- Output voltage = V_Z (constant)
- Used in power supplies to maintain constant voltage

Zener Voltage Regulation

$$V_{out} = V_Z \text{ (constant)}$$

$$R_S = (V_{in} - V_Z)/I$$

💡 Light Emitting Diode (LED)

🌟 Electroluminescence

Working Principle:

- Forward biased p-n junction
- Electrons recombine with holes
- Energy released as light photons
- $h\nu = E_g$ (band gap energy)

Materials and Colors:

- **GaAs:** Infrared
- **GaP:** Red or Green
- **GaAsP:** Red or Yellow
- **GaN:** Blue or White

Advantages:

- Low power consumption
- Long life (50,000+ hours)
- Fast switching
- No warm-up time
- Compact size

🌞 Solar Cell (Photodiode)

🌞 Photovoltaic Effect

Working Principle:

- Light photons create electron-hole pairs
- Built-in electric field separates carriers
- Converts light energy to electrical energy
- No external voltage needed

Characteristics:

- **Open circuit voltage:** 0.5 to 1 V per cell
- **Efficiency:** 15% to 20% (silicon)
- **Materials:** Si, GaAs, CdTe, CIGS
- Series/parallel combinations for higher V/I

Applications:

- Solar panels for homes
- Satellites and space stations
- Calculators and watches
- Street lights

6. JUNCTION TRANSISTOR (BJT)

Historical Background

1947: Transistor invented by Bardeen, Brattain, and Shockley at Bell Labs

1956: Nobel Prize in Physics awarded for transistor invention

Revolution: Led to modern electronics - computers, smartphones, etc.

Transistor Structure

BJT = Bipolar Junction Transistor

Called "bipolar" because both electrons and holes participate in conduction

Three Regions:

1. **Emitter (E):** Heavily doped, emits charge carriers
2. **Base (B):** Lightly doped, very thin ($\sim 10^{-6}$ m)
3. **Collector (C):** Moderately doped, collects carriers

Two Types:

- **n-p-n:** n-type emitter, p-type base, n-type collector
- **p-n-p:** p-type emitter, n-type base, p-type collector

⚡ Transistor Configuration and Biasing

🔌 Active Mode (Amplification)

For n-p-n Transistor:

- **Emitter-Base junction:** Forward biased (V_{BE} ~ 0.7 V)
- **Collector-Base junction:** Reverse biased ($V_{CB} > 0$)

Current Flow:

1. Electrons injected from emitter to base (I_E)
2. Most electrons cross thin base to collector
3. Small number recombine in base (I_B)
4. $I_E = I_C + I_B$

Transistor Current Relationship

$$I_E = I_C + I_B$$

Typically: $I_C \approx 0.95$ to $0.99\ I_E$

$I_B << I_C$ (base current very small)

📊 Current Gain Parameters

🔢 Alpha (α) and Beta (β)

1. Common Base Current Gain (α):

$$\alpha = I_C/I_E$$

Typical value: 0.95 to 0.99

Always less than 1

2. Common Emitter Current Gain (β):

$$\beta = I_C/I_B$$

Typical value: 50 to 300

Much greater than 1

Relationship between α and β:

Since $I_E = I_C + I_B$

Divide by I_E: $1 = I_C/I_E + I_B/I_E$

$1 = \alpha + I_B/I_E$

Also: $\beta = I_C/I_B = (I_E - I_B)/I_B$

⭐ **KEY RELATIONSHIPS** ⭐

$$\beta = \alpha/(1-\alpha)$$

$$\alpha = \beta/(1+\beta)$$

📈 Transistor Characteristics

📊 Input and Output Characteristics

Common Emitter Configuration (Most Used):

1. Input Characteristics (V_{BE} vs I_B):

- Plot between V_{BE} and I_B at constant V_{CE}
- Similar to diode characteristics
- Base current negligible until V_{BE} ~ 0.7 V (Si)
- **Input resistance:** $r_i = \Delta V_{BE}/\Delta I_B \sim 1\ k\Omega$

2. Output Characteristics (V_{CE} vs I_C):

- Plot between V_{CE} and I_C for different I_B values
- **Output resistance:** $r_o = \Delta V_{CE}/\Delta I_C \sim 50\ k\Omega$

Three Regions:

1. **Cut-off:** Both junctions reverse biased, $I_C \approx 0$ (OFF)
2. **Active:** E-B forward, C-B reverse (Amplification region)
3. **Saturation:** Both forward biased, I_C maximum (ON)

🔊 Transistor as Amplifier

📢 Amplification Principle

Key Concept: Small change in input controls large change in output

Common Emitter Amplifier:

- Small AC signal applied to base-emitter
- Causes small change in base current ΔI_B
- Results in large change in collector current $\Delta I_C = \beta \times \Delta I_B$
- Large output voltage across collector resistor R_C

Voltage Gain (A_v):

$$A_v = V_{out}/V_{in} = -\beta(R_C/r_i)$$

Negative sign indicates 180° phase shift

Current Gain (A_i):

$$A_i = \Delta I_C/\Delta I_B = \beta$$

Power Gain (A_p):

$$A_p = A_v \times A_i = \beta^2(R_C/r_i)$$

Transistor as Switch

Digital Operation

Two States:

1. Cut-off (OFF State - Logic 0):

- Input V_{in} = 0 V (low)
- Base current $I_B = 0$
- Collector current $I_C \approx 0$
- Output $V_{out} = V_{CC}$ (high)
- Transistor acts as open switch

2. Saturation (ON State - Logic 1):

- Input V_{in} = High
- Base current $I_B > I_{C(sat)}/\beta$
- Collector current $I_C = V_{CC}/R_C$ (maximum)
- Output $V_{out} \approx 0$ V (low)
- Transistor acts as closed switch

Switching Speed

Modern transistors: nanoseconds (10^{-9} s)
Enables GHz processors

🚪 7. DIGITAL ELECTRONICS - LOGIC GATES

🔢 Binary Logic

Digital Signals:

- **Logic 0 (LOW):** 0 V to 0.8 V
- **Logic 1 (HIGH):** 2 V to 5 V (for TTL)

Logic Gates: Building blocks of digital circuits

⚡ Basic Logic Gates

🔹 OR Gate

Boolean Expression: Y = A + B

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

Output HIGH if at least one input is HIGH

◆ AND Gate

Boolean Expression: Y = A · B or Y = AB

A	B	Y = A · B
0	0	0
0	1	0
1	0	0
1	1	1

Output HIGH only if all inputs are HIGH

◆ NOT Gate (Inverter)

Boolean Expression: Y = Ā or Y = A'

A	Y = Ā
0	1
1	0

Output is complement of input

⚡ Universal Gates

◆ NAND Gate (Universal Gate)

Boolean Expression: Y = (A · B)' = $\bar{A} + \bar{B}$ (De Morgan's Law)

A	B	Y = (AB)'
0	0	1
0	1	1
1	0	1
1	1	0

Universal: Can implement any logic function

NOT: Connect both inputs together

AND: NAND followed by NOT

OR: NAND with inverted inputs

◆ NOR Gate (Universal Gate)

Boolean Expression: $Y = (A + B)' = \bar{A} \cdot \bar{B}$ (De Morgan's Law)

A	B	Y = (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

Universal: Can implement any logic function

⚡ Special Gates

◆ XOR Gate (Exclusive OR)

Boolean Expression: $Y = A \oplus B = A'B + AB'$

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Output HIGH when inputs are different

Applications: Comparator, parity checker, adder circuits

⭐ DE MORGAN'S THEOREMS ⭐

Theorem 1:

$$(A + B)' = A' \cdot B'$$

Theorem 2:

$$(A \cdot B)' = A' + B'$$

In words:

- Complement of OR = AND of complements
- Complement of AND = OR of complements

🔌 8. INTEGRATED CIRCUITS (ICs)

🎯 What is an IC?

Definition: Complete electronic circuit (transistors, diodes, resistors, capacitors) fabricated on a single silicon chip

Advantages:

- ✅ Extremely small size (microchip)
- ✅ Low power consumption
- ✅ High reliability
- ✅ Low cost (mass production)
- ✅ High operating speed
- ✅ Easy replacement

📊 Classification by Integration Scale

Type	Full Name	Components	Example
SSI	Small Scale Integration	< 100	Logic gates (7400 series)
MSI	Medium Scale Integration	100 to 10^3	Counters, Decoders, Multiplexers
LSI	Large Scale Integration	10^3 to 10^5	Microprocessors, Memory
VLSI	Very Large Scale Integration	10^5 to 10^7	Modern processors, GPUs
ULSI	Ultra Large Scale Integration	> 10^7	Advanced processors (billions of transistors)

⚠️ 9. COMMON MISTAKES

❌ MISTAKE 1: Band Gap Confusion

Wrong: "Semiconductor has zero band gap"

Correct: Semiconductor has **small band gap (~1 eV)**

Remember: Conductor = 0, Semiconductor = ~1 eV, Insulator = >3 eV

❌ MISTAKE 2: Majority Carrier Identification

Wrong: "n-type has holes as majority carriers"

Correct: n-type = **electrons**, p-type = **holes**

Tip: n for negative (electrons), p for positive (holes)

❌ MISTAKE 3: Forward Bias Voltage

Wrong: "Diode conducts at any forward voltage"

Correct: Needs to overcome barrier: **0.7 V (Si)** or **0.3 V (Ge)**

Remember: Check the semiconductor material!

❌ MISTAKE 4: Transistor Current Relationship

Wrong: "$I_C = I_E - I_B$ is incorrect"

Correct: $I_E = I_C + I_B$ (emitter = collector + base)

Remember: Emitter current is largest, splits into collector and base

❌ MISTAKE 5: Logic Gate Truth Tables

Wrong: "AND gate output is 1 if any input is 1"

Correct: AND = **all inputs must be 1**, OR = **at least one input 1**

Tip: AND is stricter (all), OR is lenient (any)

10. PRACTICE QUESTIONS

MCQ Section

Q1. The energy gap for silicon is:

(a) 0.7 eV
(b) 1.1 eV ✓
(c) 3 eV
(d) 6 eV

Answer: (b) Si has E_g = 1.1 eV, Ge has 0.7 eV

Q2. In n-type semiconductor, majority carriers are:

(a) Holes
(b) Electrons ✓
(c) Both equally
(d) Protons

Answer: (b) n-type doped with Group V elements (extra electrons)

Q3. Barrier potential for Si p-n junction at 300 K is:

(a) 0.3 V
(b) 0.5 V
(c) 0.7 V ✓
(d) 1.1 V

Answer: (c) Si: 0.7 V, Ge: 0.3 V

Q4. In a transistor, $\beta = 100$ and $I_B = 20\ \mu A$. Then I_C is:

(a) 0.2 mA
(b) 2 mA ✓

(c) 20 mA
(d) 200 mA

Answer: (b) $I_C = \beta \times I_B = 100 \times 20\ \mu A = 2\ mA$

Q5. Which gate is called universal gate?

(a) OR
(b) AND
(c) NOT
(d) NAND ✓

Answer: (d) Both NAND and NOR are universal gates

📝 Short Answer Questions (2-3 marks)

Q6. Draw energy band diagrams for conductor, semiconductor, and insulator.

Answer:

Conductor:

- Valence and conduction bands overlap
- $E_g = 0$
- Free electrons available at all temperatures

Semiconductor:

- Small gap between VB and CB
- $E_g \sim 1$ eV
- At room temp, some electrons reach CB

Insulator:

- Large gap between VB and CB
- $E_g > 3$ eV
- Very few electrons reach CB even at high temp

Q7. Explain the formation of depletion region in p-n junction.

Answer:

Formation Process:

1. When p and n regions are joined, concentration gradient exists
2. Holes diffuse from p-side to n-side
3. Electrons diffuse from n-side to p-side

4. Recombination occurs near junction
5. p-side becomes negatively charged (acceptor ions)
6. n-side becomes positively charged (donor ions)
7. These immobile ions create depletion region
8. Electric field established opposes further diffusion
9. Equilibrium reached at barrier potential V_0

Q8. What is a Zener diode? How is it used as voltage regulator?

Answer:

Zener Diode:

- Special diode designed to operate in reverse breakdown
- Sharp breakdown at specific voltage (Zener voltage)
- Voltage remains constant in breakdown region

Voltage Regulation:

- Connected in reverse bias across load
- Series resistor R_s limits current
- When input voltage varies, Zener maintains constant V_z
- Excess voltage dropped across R_s
- Load receives constant voltage = V_z

📝 Long Answer Questions (5 marks)

Q9. Explain the working of n-p-n transistor in active mode. Derive the relation between α and β.

Answer:

Working of n-p-n Transistor:

Biasing:

- Emitter-Base junction: Forward biased (V_{BE} = 0.7 V)
- Collector-Base junction: Reverse biased (V_{CB} > 0)

Current Flow:

1. Electrons from emitter (n-type) injected into base
2. Base is thin and lightly doped
3. Most electrons (95-99%) cross base to collector
4. Only few electrons (1-5%) recombine in base
5. Strong collector field pulls electrons to collector

Relation between α and β:

Given: $I_E = I_C + I_B$

Divide by I_E: $1 = I_C/I_E + I_B/I_E$

Since $\alpha = I_C/I_E$: $1 = \alpha + I_B/I_E$

Therefore: $I_B/I_E = 1 - \alpha$

$I_B = I_E(1 - \alpha) = (I_C + I_B)(1 - \alpha)$

$I_B = I_C(1 - \alpha) + I_B(1 - \alpha)$

$I_B\alpha = I_C(1 - \alpha)$

$I_C/I_B = \alpha/(1 - \alpha)$

$\beta = \alpha/(1 - \alpha)$

Similarly: **$\alpha = \beta/(1 + \beta)$**

Q10. Explain half-wave and full-wave rectifiers with circuit diagrams. Compare their efficiencies.

Answer:

Half-Wave Rectifier:

- Uses single diode
- Converts one half cycle of AC to DC
- Other half cycle blocked
- Output: Pulsating DC (one pulse per cycle)

Full-Wave Rectifier:

- Uses two or four diodes
- Converts both half cycles to DC
- Each diode conducts alternate half cycle
- Output: Pulsating DC (two pulses per cycle)

Comparison:

Parameter	Half-Wave	Full-Wave
Efficiency	40.6%	81.2%
Ripple Factor	1.21	0.48
V_{dc}	V_m/π	$2V_m/\pi$
Frequency	f (input)	2f

Conclusion: Full-wave rectifier is superior due to higher efficiency, lower ripple, and better DC output.

🏆 11. EXAM PREPARATION

🎯 Must Master Topics

- ✨ Energy band theory and classification of materials
- ✨ Intrinsic vs extrinsic semiconductors
- ✨ p-n junction formation and depletion region
- ✨ Forward and reverse biasing
- ✨ V-I characteristics of diode
- ✨ Rectifier circuits (half-wave and full-wave)
- ✨ Zener diode voltage regulation
- ✨ Transistor working and configurations
- ✨ Transistor as amplifier and switch
- ✨ Logic gates and truth tables

💡 EXAM TIPS

For Diagrams:

- Draw energy band diagrams carefully
- Label all components in circuits
- Show polarity clearly in biasing
- Draw characteristic curves with proper axes

Common Question Types:

1. Energy band diagrams (2-3 marks)
2. p-n junction formation (3 marks)
3. Rectifier working and comparison (5 marks)
4. Transistor α and β relation (3 marks)
5. Logic gate truth tables (2 marks each)
6. V-I characteristics explanation (3 marks)

⚡ KEY FORMULAS TO REMEMBER

1. Diode Current: $I = I_0[e^{eV/kT} - 1]$

2. Transistor: $I_E = I_C + I_B$

3. Current Gains: $\alpha = I_C/I_E$, $\beta = I_C/I_B$

4. α-β Relation: $\beta = \alpha/(1-\alpha)$, $\alpha = \beta/(1+\beta)$

5. Rectifier Output: $V_{dc(HW)} = V_m/\pi$, $V_{dc(FW)} = 2V_m/\pi$

6. Efficiency: $\eta_{HW} = 40.6\%$, $\eta_{FW} = 81.2\%$

📋 Important Values to Remember

Parameter	Silicon	Germanium
Band gap	1.1 eV	0.7 eV
Barrier potential	0.7 V	0.3 V
n_i at 300 K	1.5×10^{10} cm^{-3}	2.5×10^{13} cm^{-3}

📚 Study Material Information

This comprehensive study material on **Semiconductor Electronics** (Chapter 14, Class 12 Physics) has been prepared following the latest CBSE curriculum. The content covers all essential concepts from basic semiconductors to transistors and logic gates.

EaaS - Education as a Service Model

For more resources, visit: **www.mathlove.in**

📞 **Contact Math Love Institute for personalized coaching**

🎯 **Specializing in CBSE Physics, Chemistry, Mathematics (Classes 6-12)**